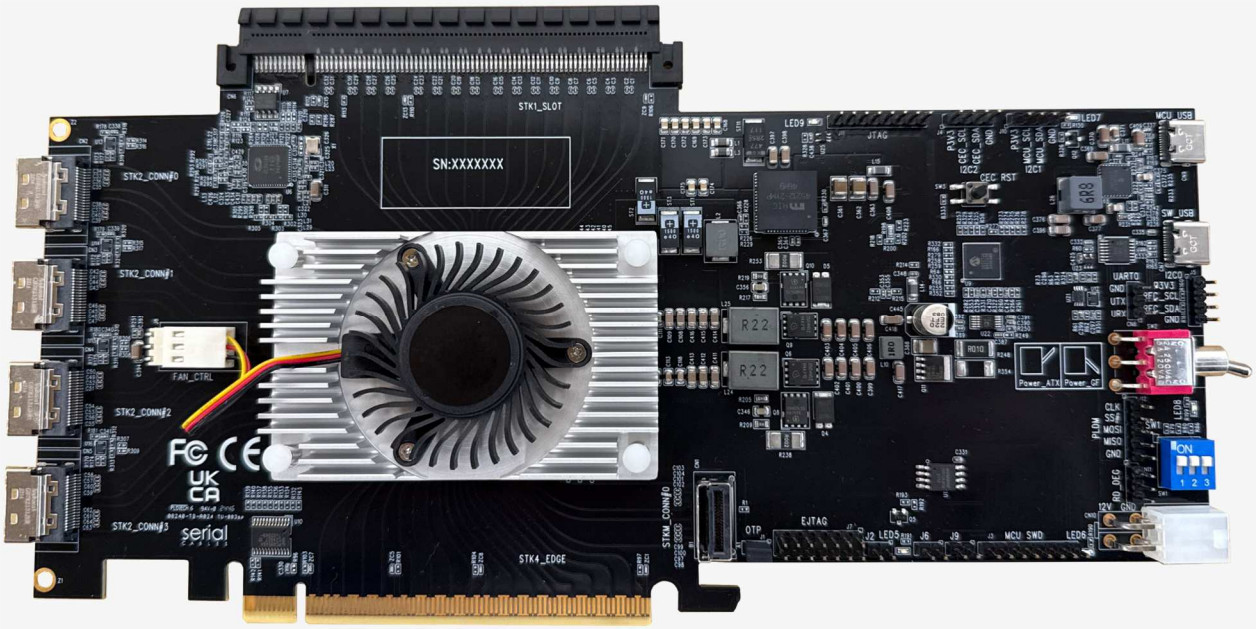
Microchip PCIe Gen5

Host Adapter Card

PCI5-AD-x16HI-MG5-52



User’s Manual

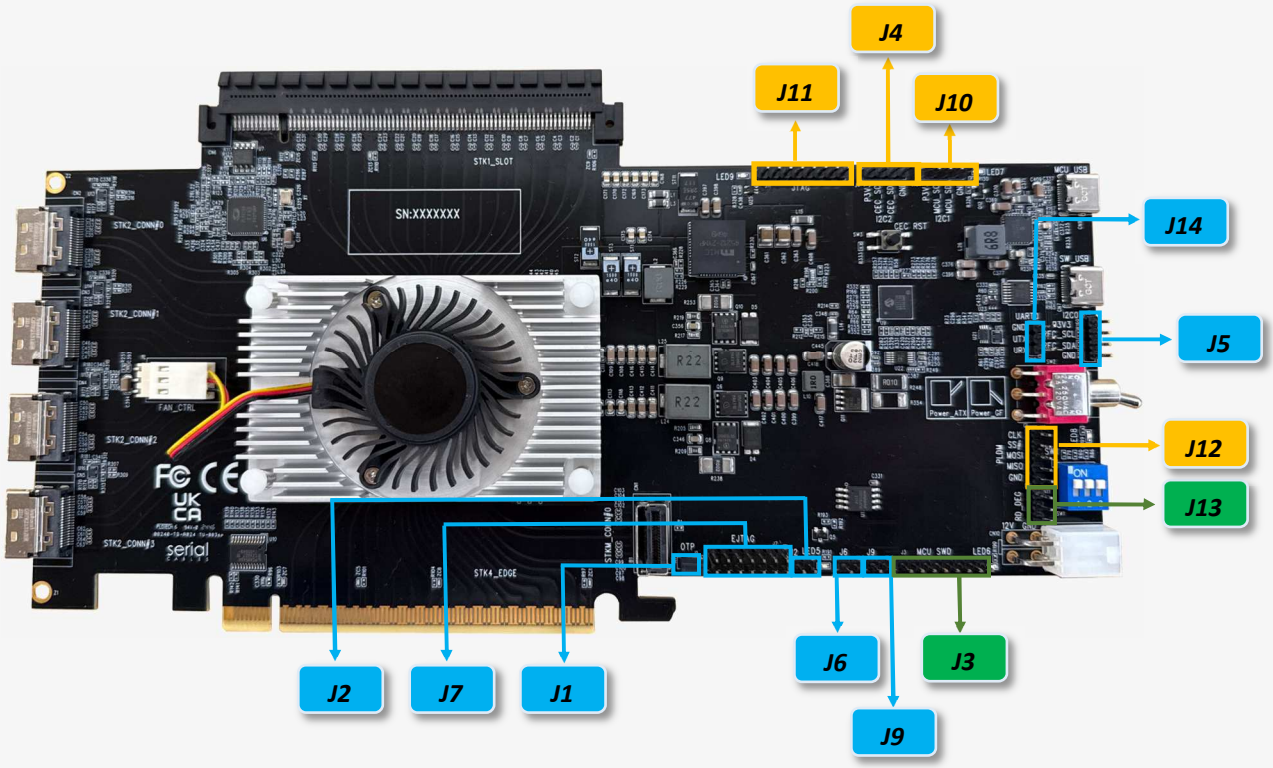
REV: 1.0

Feb. 2025

Change history

REV	Change history
Rev1.0	Preliminary released.

Function Description For Headers



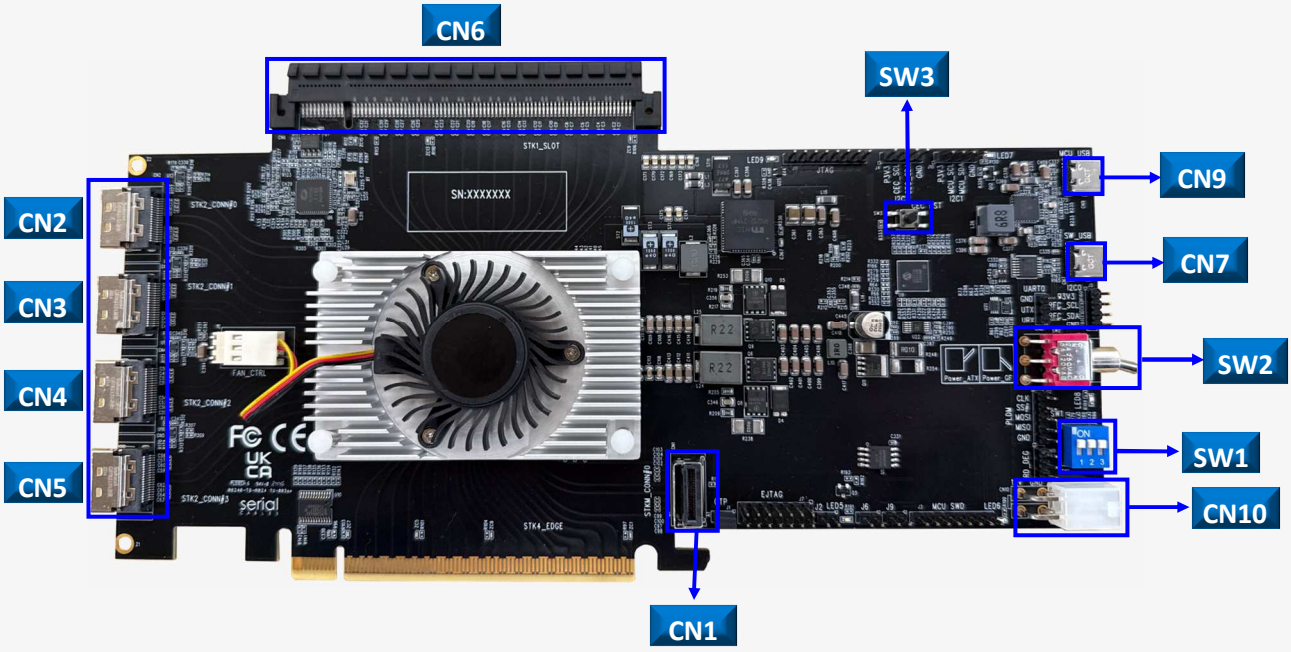
Headers for Switchtec	
J1	One-time Programmable Write Status ON: OTP memory in the switch is in read-mode.
J2	Test Debug Mode OFF: Select MIPS EJTAG mode. ON: Select normal JTAG operation.
J5	Switchtec recovery TWI port accessing
J6	Switchtec BL0 recovery mode ON: Put Switchtec into BL0 recovery mode
J9	Switchtec BL1 recovery mode ON: Put Switchtec into BL1 recovery mode
J7	14Pins EJTAG connector
J14	Switchtec and CEC1736 UART Interface

Headers for CEC1736	
J11	One-time Programmable Write Status ON: OTP memory in the switch is in read-mode.
J4	Test Debug Mode OFF: Select MIPS EJTAG mode. ON: Select normal JTAG operation.
J10	Switchtec recovery TWI port accessing
J12	PLDM Interface

Note: The CEC device is in bypass mode by default and requires additional configuration to enable

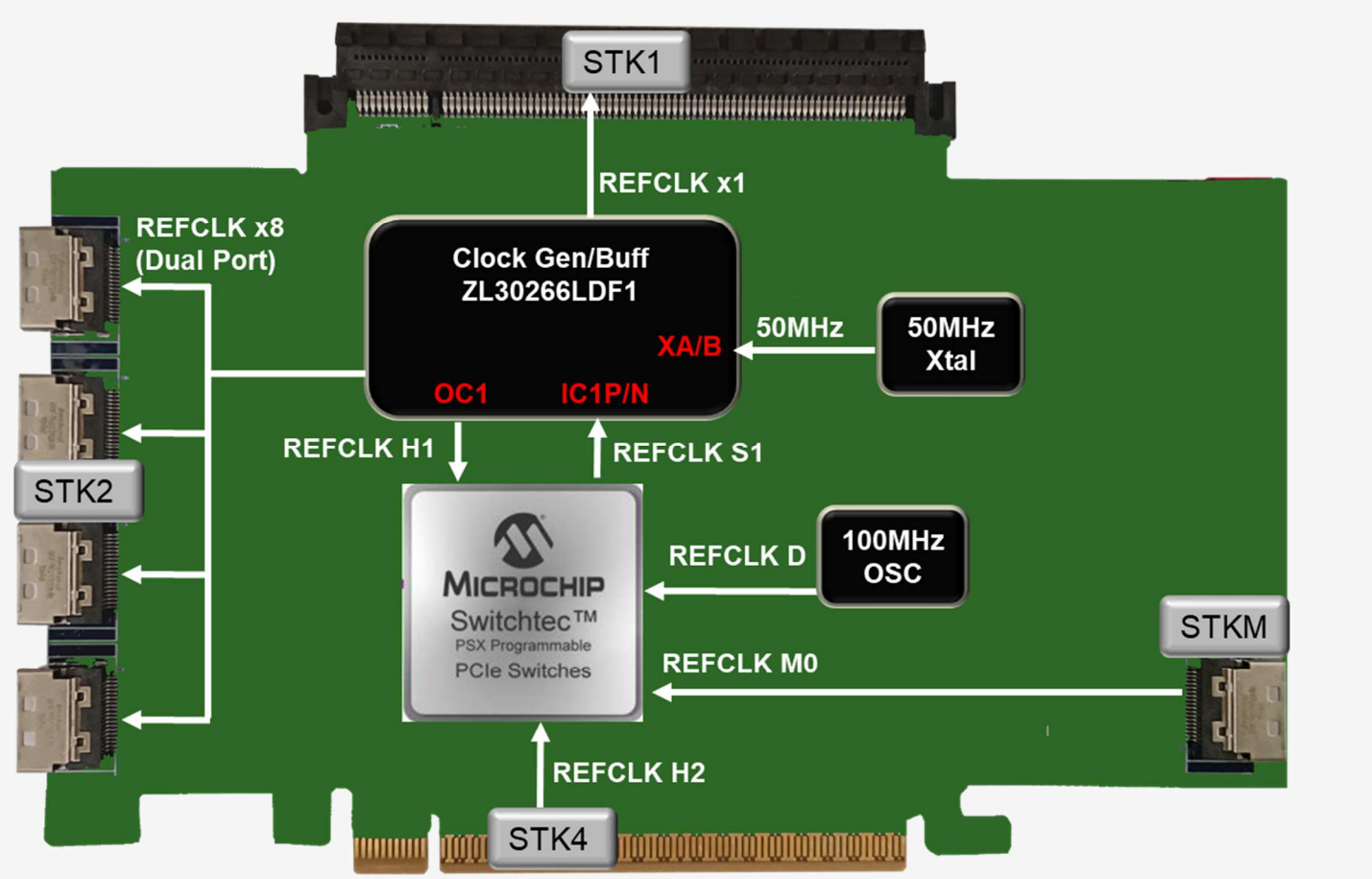
Headers for MCU SAME54	
J3	MCU Programming interface
J13	Reserve for MCU debug purpose

Function Description For Connectors



Location	Descriptions
CN1	X4 MCIO(mini-cool edge IO), SFF-TA-1016 connector. SFF9402 end-point pinout. Reserved as management port for further used.
CN2:CN5	X4 MCIO(mini-cool edge IO), SFF-TA-1016 connector. SC pinout
CN6	PCIe Gen5 X16 Straddle connector.
CN7	Type-C USB connector for CEC1736 UART interface or Switchtec recovery interface.
CN9	Type-C USB connector for MCU SAME54 running CLI commands.
CN10	ATX4Pin Power connector
SW2	Toggle switch for input power select, coming from either golden finger or ATX4Pins connector.
SW1	Switchtec bifurcation mode selection
SW3	reset button for CEC1736

Stack Allocation And Clock Diagram



Switchtec Bifurcation Selection (SW1)

Modes	SW1	Bifurcation Stack 1 (STR)	Bifurcation Stack 2 (MCIO)	Clocking Setting	Clock Gen Config AC[2:0]
Mode 1 4x4 CC		1x16	4x4	SKT1: CC/[CLK_H2] SKT2: CC/[CLK_H2] SKT4: CC/[CLK_H2] SKTM: CC/[CLK_M0]	001: All output HCSL no SSC, sourced by IC1P/N (REFCLK_H2 for CC)
Mode 2 8x2 CC		1x16	8x2		
Mode 3 4x4 SRNS		1x16	4x4	SKT1: CC/[CLK_H2] SKT2: SRNS/[CLK_H1] SKT4: CC/[CLK_H2] SKTM: CC/[CLK_M0]	010: All output HCSL no SSC, sourced by IC1P/N (REFCLK_H2 for CC) Switchtec and straddle port to be CC Disable clock in MCIO port for SRNS testing
Mode 4 8x2 SRNS		1x16	8x2		
Mode 5 4x4 SRIS		1x16	4x4	SKT1: CC/[CLK_H2] SKT2: SRIS/[CLK_H1] SKT4: CC/[CLK_H2] SKTM: CC/[CLK_M0]	100: All output HCSL, sourced by IC1P/N (REFCLK_H2 for CC) Switchtec to be 3,000ppm SSC for Gen5 SRIS Straddle port to be CC Disable clock in MCIO port for SRIS testing
Mode 6 8x2 SRIS		1x16	8x2		
Mode 7 4x4 CC		1x16	4x4	SKT1: CC/[CLK_D] SKT2: CC/[CLK_D] SKT4: CC/[CLK_D] SKTM: CC/[CLK_M0]	111: All outputs HCSL with no SSC, Sourced by 50MHz Crystal
Mode 8 1x16		1x16	1x16	SKT1: CC/[CLK_H2] SKT2: CC/[CLK_H2] SKT4: CC/[CLK_H2] SKTM: CC/[CLK_M0]	001: All output HCSL no SSC, sourced by IC1P/N (REFCLK_H2 for CC)

Note:

Mode 1 and 2 are “common clock” with 4x4 and 8x2 bifurcations in MCIO ports.

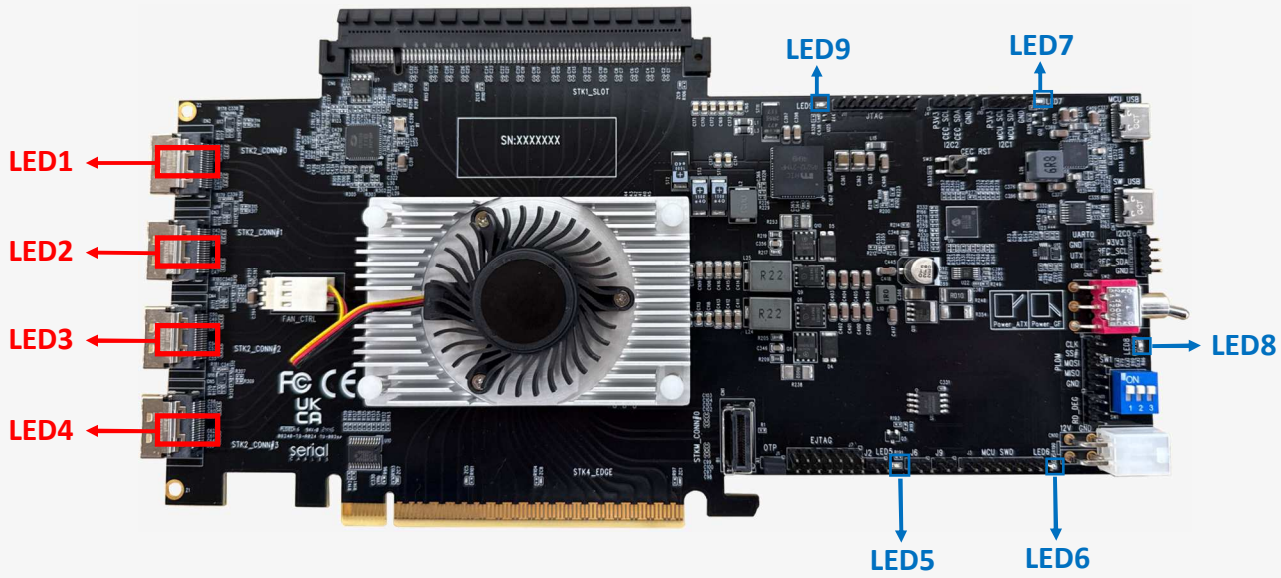
Mode 3 and 4 are “SRNS” with 4x4 and 8x2 bifurcations in MCIO ports.

Mode 5 and 6 are “SRIS” with 4x4 and 8x2 bifurcations in MCIO ports.

Mode 7 is similar to Mode 1, the only difference is changing the clock source of clock buffer from local Xtal instead of golden finger.

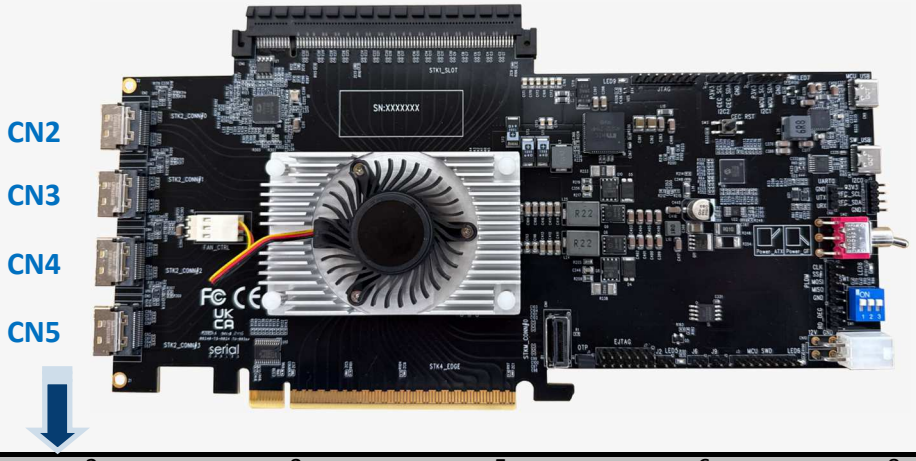
Mode 8 is to set 1x16 bifurcation in MCIO ports and used to connect MCIO to PCIe 1x16 slot adapter card.

Function Description For LEDs



Location	Color	Description
LLED6	Green	**Host card Healthy LED** Blinking: Host adapter card working correctly. Solid ON: Any failure events detected, etc. voltages, FAN, and temperatures failed
LED5	Blue	**Switchtec Heartbeat LED** Blinking: Switchtec working correctly. Solid ON: Any errors detected in boot-Loader, Switchtec FW or HW.
LED8	Blue	Host card P12V power LED
LED7	Green	CEC1736 status LED
LED9	Red	ON: fatal error detected in CEC1736
LED1/2/3/4	Red	**MCIO Port link matching LEDs** In Mode [1:7]: Each LED corresponds to MCIO port. LED1, LED2, LED3 and LED4 light when attached devices in MCIO port not link at x4 or 2x2 link width. In mode 8: LED1 lights when connected device in MCIO port not link at 1x16 link width.

MCIO Pins Definition



		2	3	5	6	8	9
CN2	A	PCIE_S2_RX0_P	PCIE_S2_RX0_N	PCIE_S2_RX1_P	PCIE_S2_RX1_N	MCIO_CLK1R_N	MCIO_CLK1R_P
	B	PCIE_S2_TX0_P	PCIE_S2_TX0_N	PCIE_S2_TX1_P	PCIE_S2_TX1_N	MCIO_CLK6R_N	MCIO_CLK6R_P
		14	15	17	18	11	12
	A	PCIE_S2_RX2_P	PCIE_S2_RX2_N	PCIE_S2_RX3_P	PCIE_S2_RX3_N	MCIO_SCL0	MCIO_SDA0
	B	PCIE_S2_TX2_P	PCIE_S2_TX2_N	PCIE_S2_TX3_P	PCIE_S2_TX3_N	MCIO_RST#_0	MCIO_RST#_1

		2	3	5	6	8	9
CN3	A	PCIE_S2_RX4_P	PCIE_S2_RX4_N	PCIE_S2_RX5_P	PCIE_S2_RX5_N	MCIO_CLK3R_N	MCIO_CLK3R_P
	B	PCIE_S2_TX4_P	PCIE_S2_TX4_N	PCIE_S2_TX5_P	PCIE_S2_TX5_N	MCIO_CLK4R_N	MCIO_CLK4R_P
		14	15	17	18	11	12
	A	PCIE_S2_RX6_P	PCIE_S2_RX6_N	PCIE_S2_RX7_P	PCIE_S2_RX7_N	MCIO_SCL1	MCIO_SDA1
	B	PCIE_S2_TX6_P	PCIE_S2_TX6_N	PCIE_S2_TX7_P	PCIE_S2_TX7_N	MCIO_RST#_2	MCIO_RST#_3

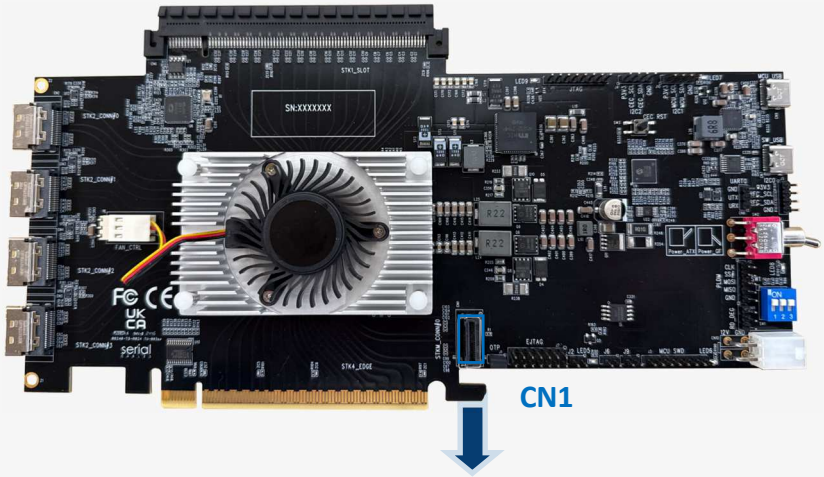
		2	3	5	6	8	9
CN4	A	PCIE_S2_RX8_P	PCIE_S2_RX8_N	PCIE_S2_RX9_P	PCIE_S2_RX9_N	MCIO_CLK5R_P	MCIO_CLK5R_N
	B	PCIE_S2_TX8_P	PCIE_S2_TX8_N	PCIE_S2_TX9_P	PCIE_S2_TX9_N	MCIO_CLK2R_N	MCIO_CLK2R_P
		14	15	17	18	11	12
	A	PCIE_S2_RX10_P	PCIE_S2_RX10_N	PCIE_S2_RX11_P	PCIE_S2_RX11_N	MCIO_SCL2	MCIO_SDA2
	B	PCIE_S2_TX10_P	PCIE_S2_TX10_N	PCIE_S2_TX11_P	PCIE_S2_TX11_N	MCIO_RST#_4	MCIO_RST#_5

		2	3	5	6	8	9
CN5	A	PCIE_S2_RX12_P	PCIE_S2_RX12_N	PCIE_S2_RX13_P	PCIE_S2_RX13_N	MCIO_CLK7R_P	MCIO_CLK7R_N
	B	PCIE_S2_TX12_P	PCIE_S2_TX12_N	PCIE_S2_TX13_P	PCIE_S2_TX13_N	MCIO_CLK0R_N	MCIO_CLK0R_P
		14	15	17	18	11	12
	A	PCIE_S2_RX14_P	PCIE_S2_RX14_N	PCIE_S2_RX15_P	PCIE_S2_RX15_N	MCIO_SCL3	MCIO_SDA3
	B	PCIE_S2_TX14_P	PCIE_S2_TX14_N	PCIE_S2_TX15_P	PCIE_S2_TX15_N	MCIO_RST#_6	MCIO_RST#_7

Note: Host card supports 3 types of side-band modes (SC,ACE, and ACU).

The sideband signals listed in table above as mark in yellow are for SC side-band mode.

MCIO Pins Definition (cont.)



CN1		2	3	5	6	8	9
	A	PCIE_SM_RX0_P	PCIE_SM_RX0_N	PCIE_SM_RX1_P	PCIE_SM_RX1_N	MCU_MAN_SCL	MCU_MAN_SDA
	B	PCIE_SM_TX0_P	PCIE_SM_TX0_N	PCIE_SM_TX1_P	PCIE_SM_TX1_N	NC	NC
		14	15	17	18	11	12
	A	PCIE_SM_RX2_P	PCIE_SM_RX2_N	PCIE_SM_RX3_P	PCIE_SM_RX3_N	MAG_PERST#	GND
	B	PCIE_SM_TX2_P	PCIE_SM_TX2_N	PCIE_SM_TX3_P	PCIE_SM_TX3_N	MAG_CLK_P	MAG_CLK_N

Side-band Signals in MCIO ports

Pin	SC mode	ACE mode	ACU mode
A8	MCIO_CLK1R_N		
A9	MCIO_CLK1R_P		
B8	MCIO_CLK6R_N	PWRDIS	PWRDIS
B9	MCIO_CLK6R_P	HOST_LED	LINKFAT
A11	MCIO_SCL0		
A12	MCIO_SDA0		
B11	MCIO_RST#_0		
B12	MCIO_RST#_1		

SC: Serial cables mode

Use for drive direct attached via MCIO cables, support single port U2/U3 and dual ports U2/U3 cables.

visit the website below for more details in cables support

https://serialcables.com/category/pcie-gen5/gen5-cables-183

ACE: Adapter Card EDSFF

Using MCIO to MCIO cables connect with “MCIO to EDSFF adapter card”.

a.) it supports PWRDIS command in CLI for attached EDSFF drives in MCIO ports.

b.) it supports HLED commands in CLI for attached EDSFF drives in MCIO ports.

ACU: Adapter Card U2

Use MCIO to MCIO cable to connect with “MCIO to U2 adapter card”.

a.) it supports PWRDIS command in CLI for attached U.2 drives in MCIO ports.

[Switchtec host card]

[MCIO to MCIO cable]

[MCIO to U2 adapter]

U.2 single/dual port drives

[MCIO to EDSFF adapter]

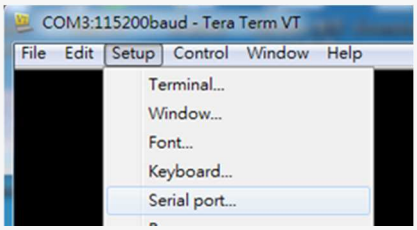
E.1L, E1.S, E3 drives

MCU CLI Setup

Step2: Tera-term setting

Step 1. Install and launch Tera Term application
(or Hyper Terminal requires version 3.0 or higher).

Step 2: To ensure proper communications between host adapter card and the VT100 Terminal emulation, please configure the VT100 Terminal emulation settings to the values shown below:



Step 3:

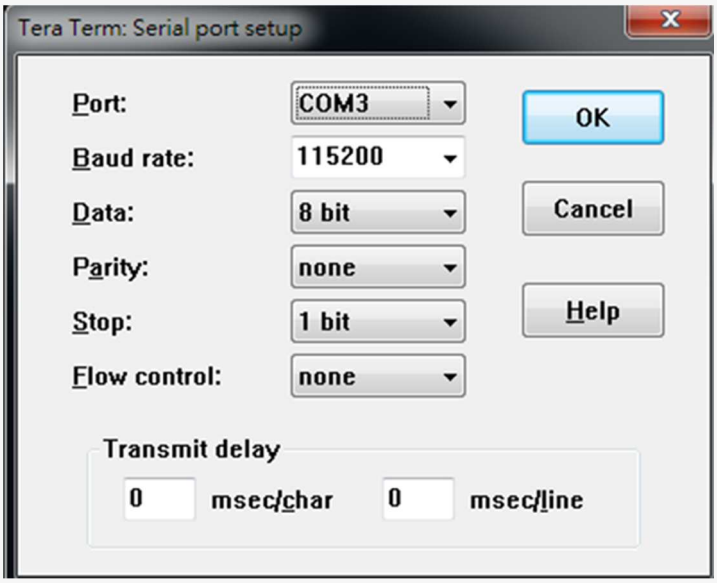
For “Port”, select COM3 in this example. (Depend on which COM port used on Host)

For “Baud rate”, select 115200.

For “Data”, select 8 bit. For “Parity”, select none.

For “Stop”, select 1 bit. For “Flow control”, select: none.

Click OK when you have finished your selections.



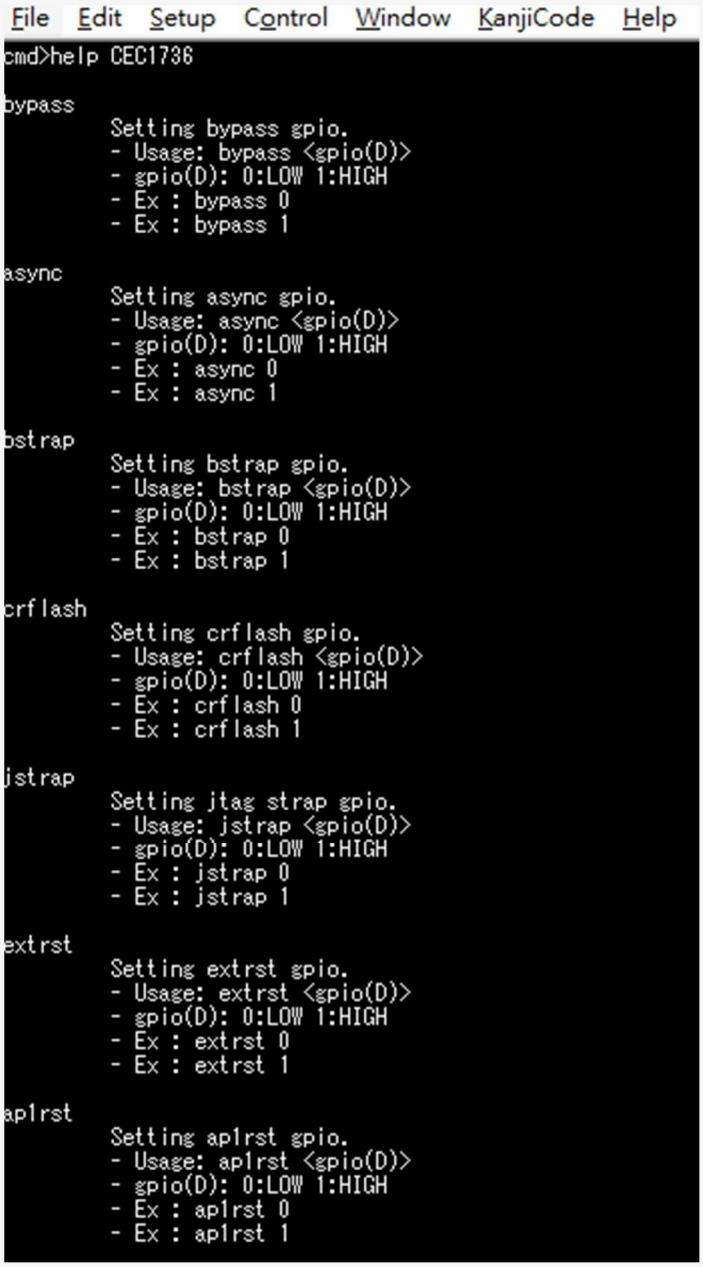
MCU Commands List

Commands	Description
CEC1736	Commands for trust controller CEC1736 GPIO setting
fdl	Update the configuration file or firmware for Switchtec and MCU FW upgrading
lsd	Shows both of switchtec and board temperatures, FAN speed, voltages and Side-band modes.
ssdrst	Issue 300ms duration PERST# to attached devices in MCIO ports and straddle PCIe connector.
showport	Shows link status for USP in golden finger, DSP for MCIO ports and Straddle port.
showmode	shows Switchtec bifurcation mode in operating.
clksel	select the mode of clock generator/buffer.
usel	Select the UART0 in header J14 comes from CEC1736 or Switchtec.
sbsel	Select the side-band mode in MCIO ports to be SC, ACE, ACU or others.
iicwr	SMBus data read from drive attached in MCIO ports or PCIe straddle port.
iicw	SMBus data write to drive attached in MCIO ports or PCIe straddle port.
ver	Shows host card information, MCU, Switchtec FW and config version.
reset	MCU FW reset (not including Switchtec reset).
swreset	sending fundamental reset to Switchtec.
sysinfo	Show all of information in Microchip host card.
pwrdis	Set PWRDIS to H state (disable SSD power), or L state (enable SSD power)
hled	Turn ON/OFF the host LED inside EDSFF drive

[CEC1736 Command Group]

Following commands are used for CEC1736 GPIO setting.

-Usage: help CEC1736



[CEC1736 Command Group]

bypass Command

Setting bypass gpio.

- Usage: bypass <gpio(D)>

- gpio(D): 0:LOW 1:HIGH

async Command

Setting async gpio.

- Usage: async <gpio(D)>

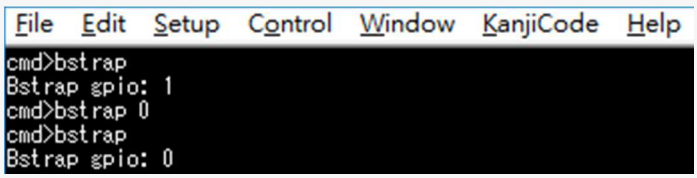
- gpio(D): 0:LOW 1:HIGH

bsatrap Command

Setting bstrap gpio.

- Usage: bstrap <gpio(D)>

- gpio(D): 0:LOW 1:HIGH

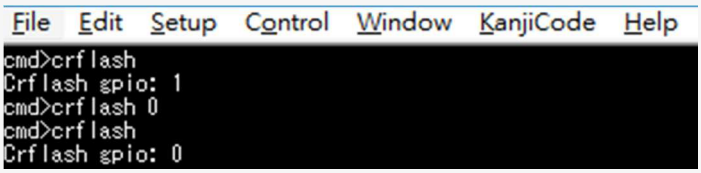


crflash Command

Setting crflash gpio.

- Usage: crflash <gpio(D)>

- gpio(D): 0:LOW 1:HIGH



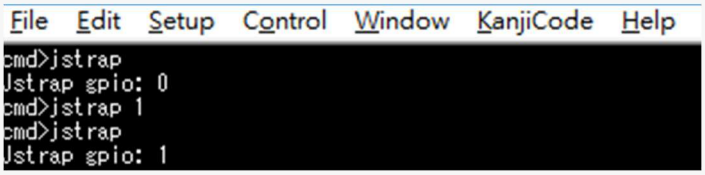
[CEC1736 Command Group]

Jstrap Command

Setting jtag strap gpio.

- Usage: jstrap <gpio(D)>

- gpio(D): 0:LOW 1:HIGH

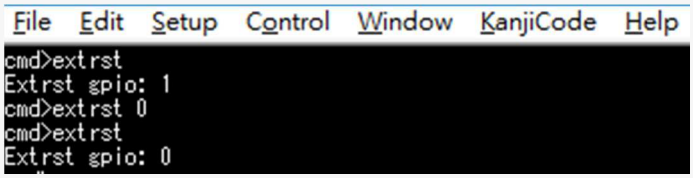


extrst Command

Setting extrst gpio.

- Usage: extrst <gpio(D)>

- gpio(D): 0:LOW 1:HIGH

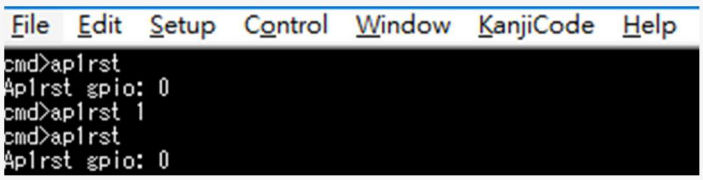


ap1rst Command

Setting ap1rst gpio.

- Usage: ap1rst <gpio(D)>

- gpio(D): 0:LOW 1:HIGH

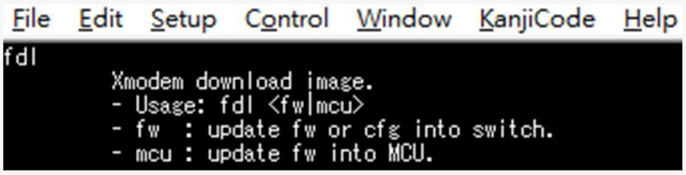


fdl Command

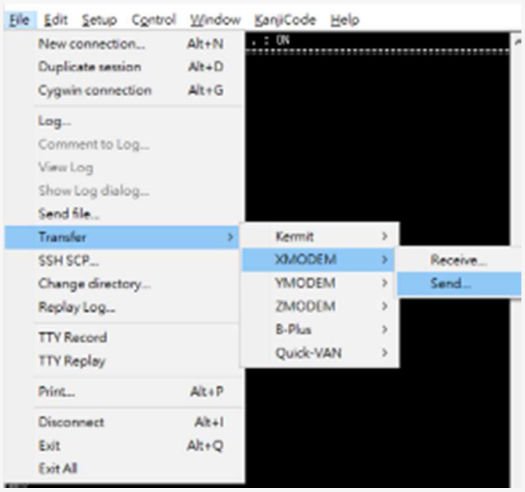
1. Update the configuration file or firmware for Switchtec

2. on-board MCU FW upgrading

-Usage: fdl |fw|MCU



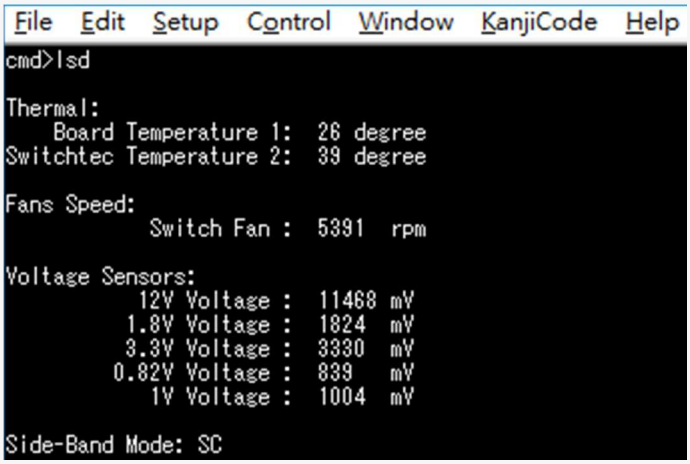
Sending upgrading file via XMODEM



lsd Command

Shows both of switchtec and board temperatures, FAN speed, voltages and Side-band modes.

-Usage: lsd



Thermal:

Board Temperature is the sensor near Switchtec.

Switchtec temperature is the sensor inside Switchtec PCIe switch.

Fan Speed: FAN RPM value reading.

Voltage sensors: Main voltages monitoring in Microchip host adapter card.

Side-Band Mode: Shows running side-band mode.

ssdrst Command

Issue 300ms duration PERST# to attached devices in MCIO ports and straddle PCIe connector.

-Usage: ssdrst <con(D)|all> [channel(C)]

-con(D) : con number should be 0 ~ 4

-channel(C) : channel number should be a or b

```
File  Edit  Setup  Control  Window  KanjiCode  Help
Cmd>ssdrst 1
Reset con 1 success
Cmd>
```

Issue PERST# signals in MCIO CON1.

```
File  Edit  Setup  Control  Window  KanjiCode  Help
Cmd>ssdrst all
Reset all con success
```

Issue PERST# signals in MCIO CON0 to CON3 and PCIe straddle connector CON4.

```
File  Edit  Setup  Control  Window  KanjiCode  Help
Cmd>ssdrst 1 a
Reset channel a of con 1 success
```

Issue PERST# signals in MCIO CON1 for channel A.

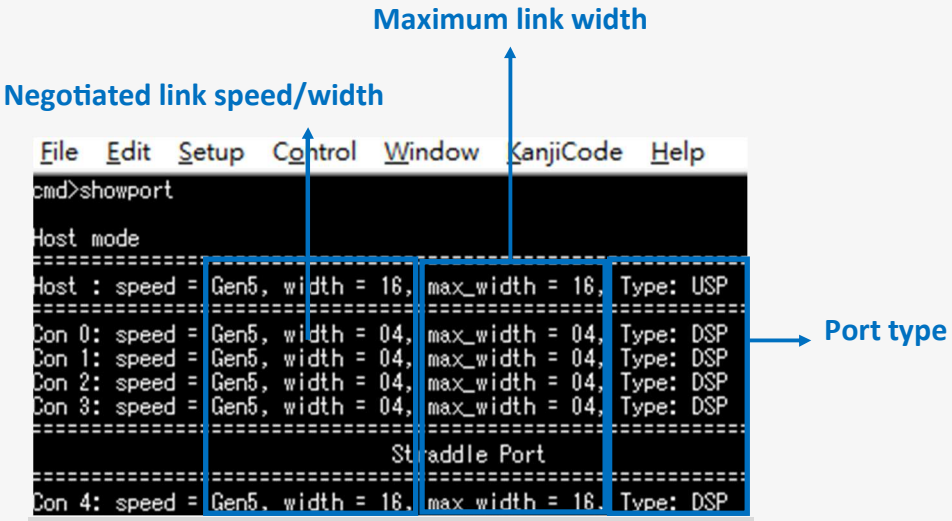
CON Mapping

showport Command

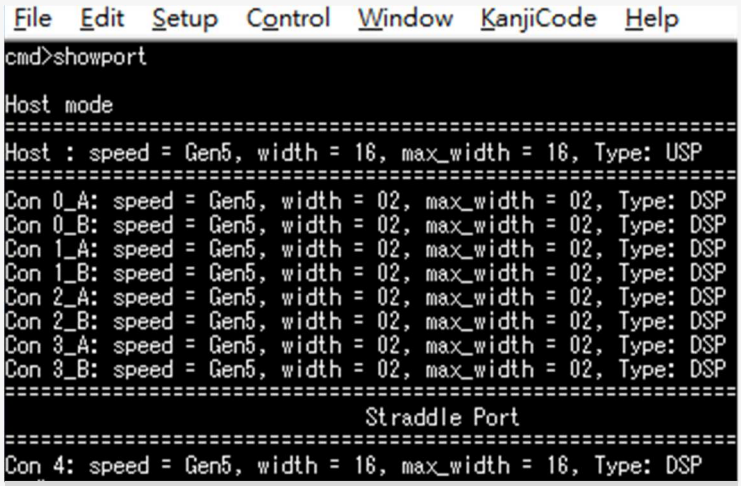
Shows link status for USP in golden finger, DSP for MCIO ports and straddle port.

-Usage: showport

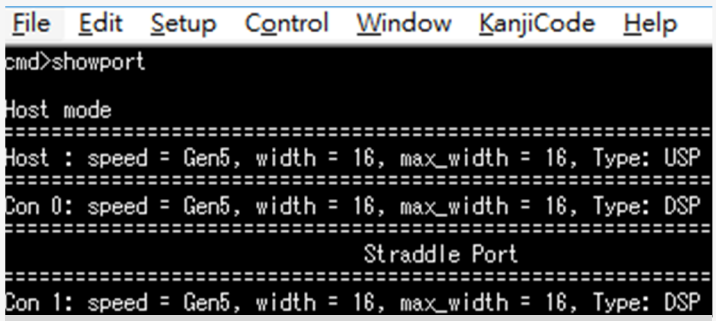
Refer to page 19 for CON number mapping.



Examples for Mode 1, 3, 5 and 7.



Examples for Mode 2, 4 and 6.



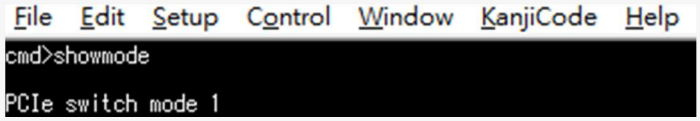
Examples for Mode 7.

Showmode Command

shows Switchtec bifurcation mode in operating.

- Usage: showmode

Refer to page 7 for bifurcation modes in Microchip Gen5 host adapter card.



clksel Command

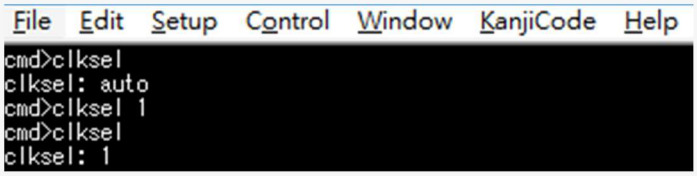
select the mode of clock generator/buffer.

- Usage: clksel <mode(D)|auto>

- mode(D): 0 ~ 7

- Ex : clksel 0

- Ex : clksel 1



The default setting is auto for “clock mode”. Refer to page 7 for the combinations of bifurcation and clock mode default setting.

Clock Mode	Description
0	All outputs HCSL with no SSC, Sourced by 50MHz Crystal
1	All outputs HCSL with no SSC, Sourced by 1C1P/N for Common-Clock
2	All output HCSL no SSC, sourced by IC1P/N (REFCLK_D for CC) Switchtec and straddle port to be CC Disable clock in MCIO port for SRNS testing
3	All output HCSL no SSC, sourced by IC1P/N (REFCLK_D for CC) Switchtec to be 5,000ppm SSC for Gen4 SRIS Straddle port to be CC Disable clock in MCIO port for SRIS testing
4	Output HCSL with no SSC, sourced by IC1P/N (REFCLK_D for CC) Switchtec to be 3,000ppm SSC for Gen5 SRIS Straddle port to be CC Disable clock in MCIO port for SRIS testing
5	Output HCSL with IC1 to be the source for OC1 and OC2, and 50MHz Crystal to be source for OC3-OC10 with SSC
6	All outputs HCSL with SSC, Sourced by 50MHz Crystal
7	All outputs HCSL with no SSC, Sourced by 50MHz Crystal

usel Command

Select the Uart0 in header J14 comes from Switchtec(default) or CEC1736.

- Usage: usel <select(D)>

- select(D): 0:Uart for Switchtec, 1:Uart for CEC1736

- Ex : usel 0

- Ex : usel 1

sbsel Command

Select the side-band mode to be SC(default), ACE, ACU or others.

- Usage: sbsel <select(D)>

- select(D): 0:SC, 1:ACE, 2:ACU

- Ex : sbsel 0

- Ex : sbsel 1

Refer to page 11 for details of side-band mode.

iicwr Command

SMBus data read from drive attached in MCIO ports and straddle connector.

-Usage: iicwr <Addr(H)> <con(D)> <ReadByte(D)> <WriteData(H)>

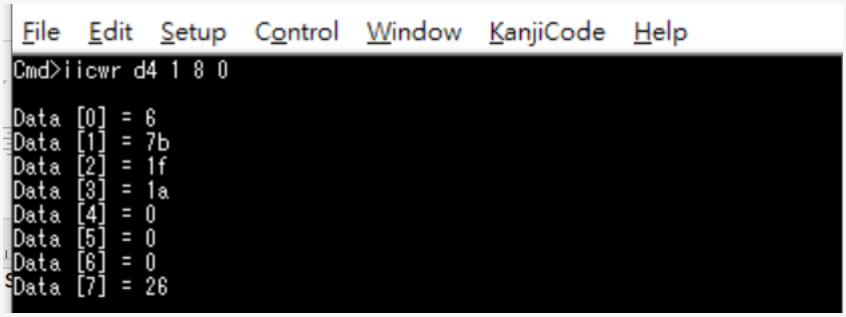
-Addr(H) : Device address

C-on(D) : Con should be 0 ~ 4

-ReadByte(D) : Max read byte is 32 byte

-WriteData(D) : Max write byte is 32 byte

Ex : iicwr d4 1 8 0



Read 8 bytes data starts from register “0” of I2C slave address “0xd4” in drive which attaches in MCIO CON1.

Refer to page 19 for CON number mapping.

iicw Command

SMBus data write to drive attached in MCIO ports and straddle connector.

-Usage: iicw <Addr(H)> <conD)> <WriteData(H)...>

-Addr(H) : Device address

-con(D) : Con should be 0 ~ 4

-WriteData(D) : Max write byte is 128 byte

Ex : iicw d4 1 ff

Write data “0xff” to I2C slave address “0xd4” in drive which attaches in MCIO CON 1.

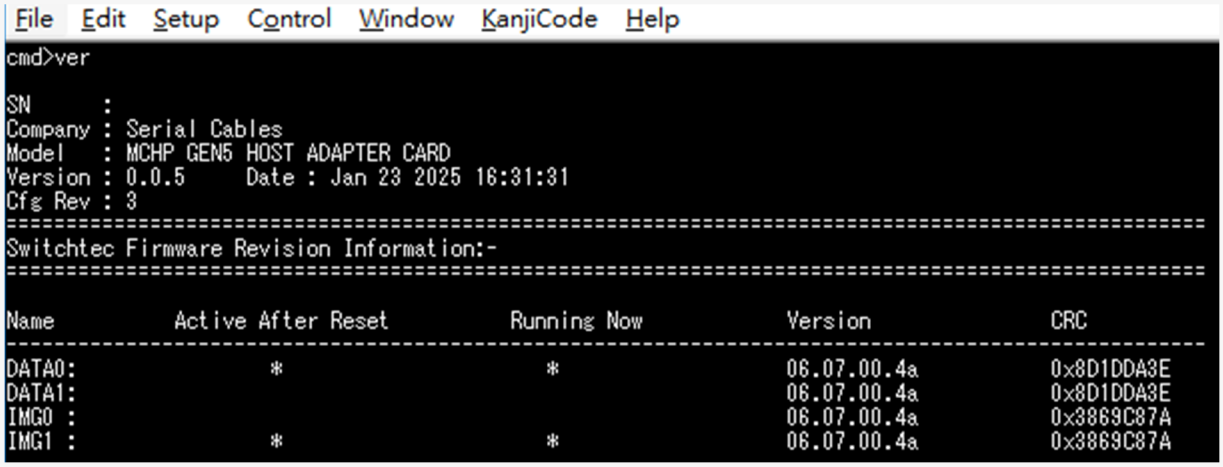
Refer to page 19 for CON number mapping.

ver Command

Shows Serial Number, company information, model name, MCU FW and MCHP FW/config version,

Also, the running image and config file version.

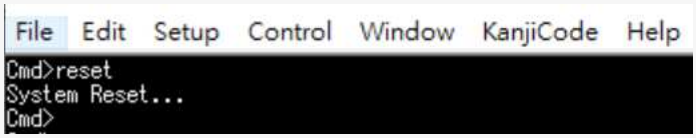
- Usage: ver



reset Command

Reset MCU

-Usage: reset



reset command is used to reset MCU only, won't reset Switchtec.

swreset Command

PCIe switch reset.

- Usage: bist

swreset command is used to Switchtec only, won't reset MCU.

sysinfo Command

Show all of information in Microchip host card.

Sysinfo command is for host card status checking, it combines series of commands including ver, lsd, and showport.

- Usage: sysinfo

```
File  Edit  Setup  Control  Window  KanjiCode  Help
cmd>sysinfo

================================================================================
ver
================================================================================

SN      :
Company : Serial Cables
Model   : MCHP GEN5 HOST ADAPTER CARD
Version : 0.0.5     Date : Jan 23 2025 16:59:55
Cfg Rev : 3
================================================================================================================
Switchtec Firmware Revision Information:-
================================================================================================================

Name          Active After Reset          Running Now           Version              CRC
----------------------------------------------------------------------------------------------------------------
DATA0:                *                       *                 06.07.00.4a          0x8D1DDA3E
DATA1:                                                          06.07.00.4a          0x26257893
IMG0 :                                                          06.07.00.4a          0x3869C87A
IMG1 :                *                       *                 06.07.00.4a          0x3869C87A


================================================================================
lsd
================================================================================

Thermal:
    Board Temperature 1:  31 degree
Switchtec Temperature 2:  41 degree

Fans Speed:
           Switch Fan :  6403  rpm

Voltage Sensors:
          12V Voltage :  11616 mV
         1.8V Voltage :  1804  mV
         3.3V Voltage :  3316  mV
        0.82V Voltage :  829   mV
          1V Voltage :  1001  mV

Side-Band Mode: SC


================================================================================
showport
================================================================================

Host mode
============================================================================
Host : speed = Gen5, width = 08, max_width = 16, Type: USP
============================================================================
Con 0: speed = Gen1, width = 00, max_width = 04, Type: DSP
Con 1: speed = Gen1, width = 00, max_width = 04, Type: DSP
Con 2: speed = Gen1, width = 00, max_width = 04, Type: DSP
Con 3: speed = Gen1, width = 00, max_width = 04, Type: DSP
============================================================================
                          Straddle Port
============================================================================
Con 4: speed = Gen1, width = 00, max_width = 16, Type: DSP
```

pwrdis Command (Applicable in ACE and ACU modes)

Set the signal level of pwrdis in MCIO connectors to be high or low.

- Usage: pwrdis [<con(D)|all> <h/l>(C)]

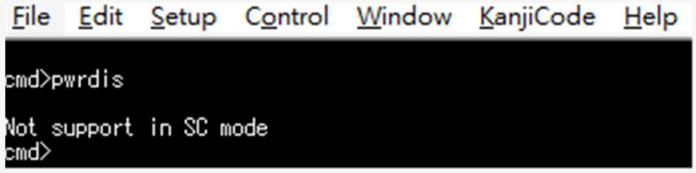
- con(D) : con number should be 0 ~ 3

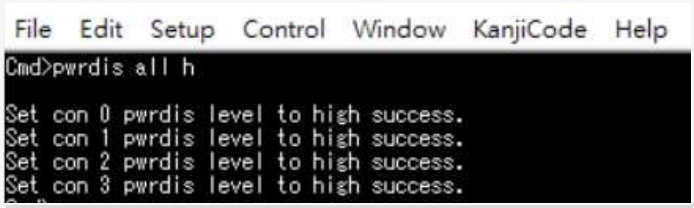
- h(C) : disable SSD power

- l(C) : enable SSD power

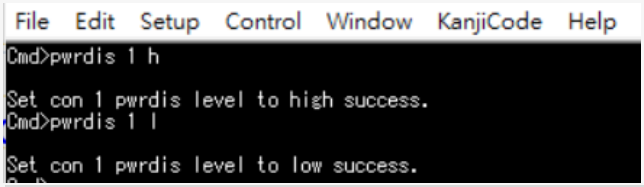
- Ex : pwrdis all h

- Ex : pwrdis 1 h





Set PWRDIS to “H” state in all of MCIO ports



Set PWRDIS to “H” or “L” state in MCIO port 1

hled Command (Applicable in ACE mode)

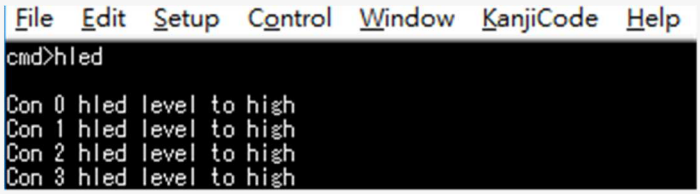
Set hled signals in EDSFF SSD to be on or off.

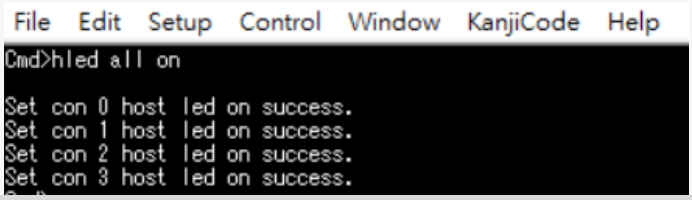
- Usage: htled <con(D)|all> <on|off>

- con(D) : con number should be 0 ~ 3

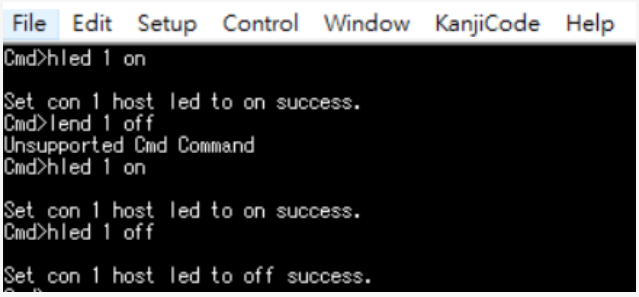
- Ex : hled all on

- Ex : hled 1 on





Turn on all of host LEDs in EDSFF drives.



Turn ON/OFF host LED in EDSFF drive which attached in MCIO port1