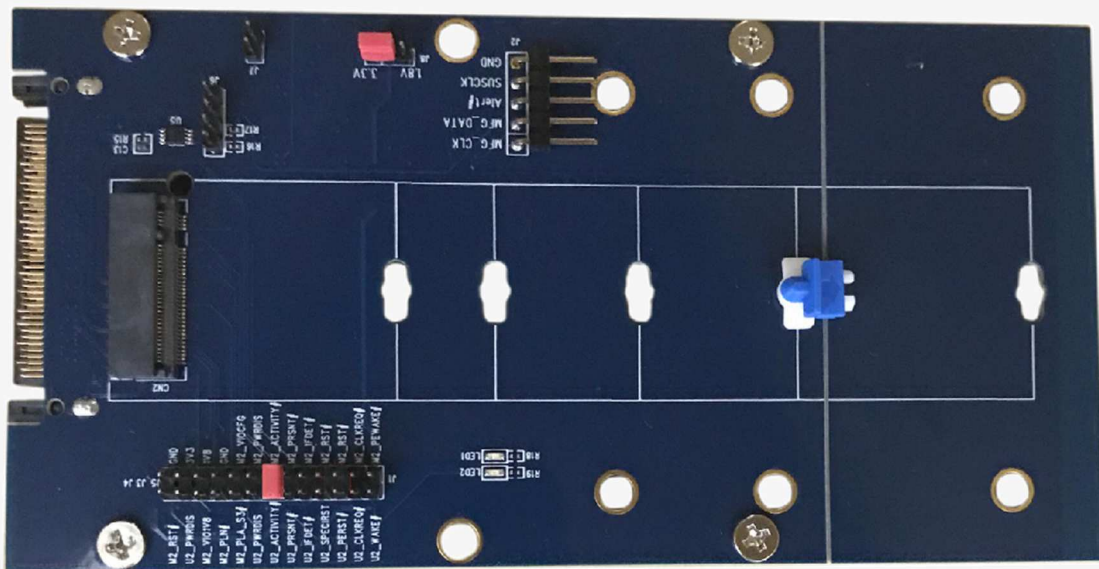




serial
C A B L E S

PCIe Gen5 U.2 To M.2 Adapter Card

Part Number: PCI5-AD-U2M2-04



User's Manual

REV: 1.2

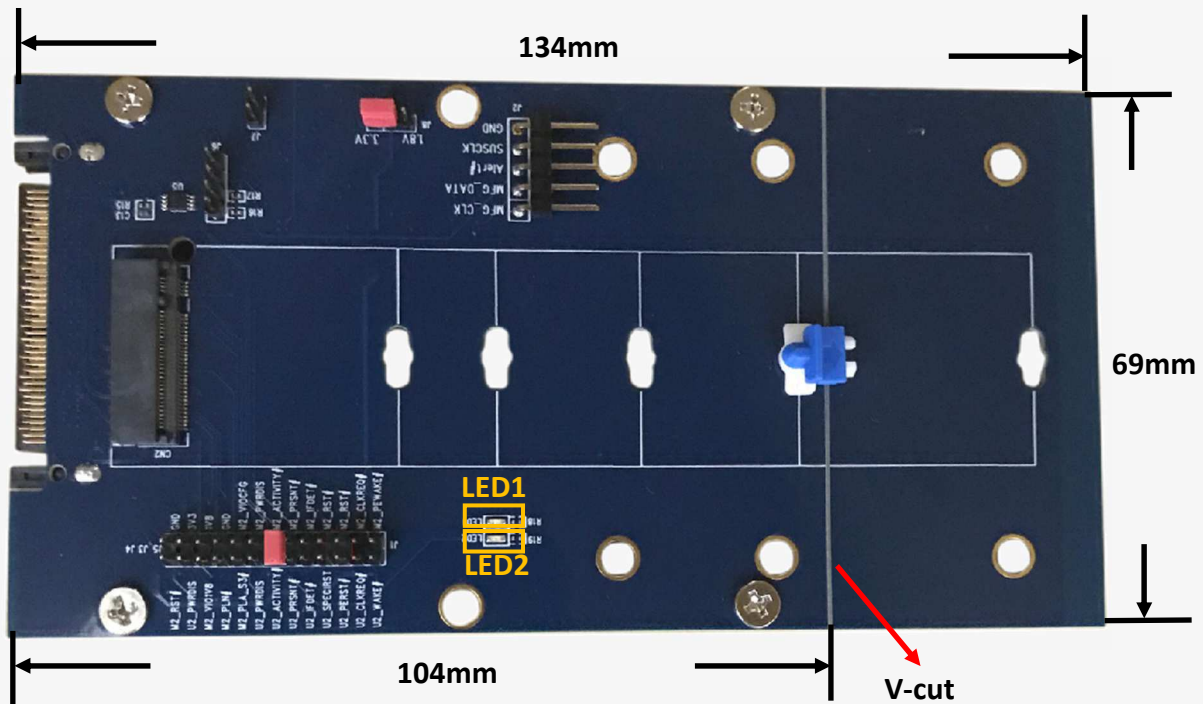
April. 2024



Change history

REV	Change history	Date of Release
1.0	New created	Dec. 2022
1.1	Updated the default jumper setting	Aug.2023
1.2	Added descriptions for pin headers	Apr. 2024

Product Brief

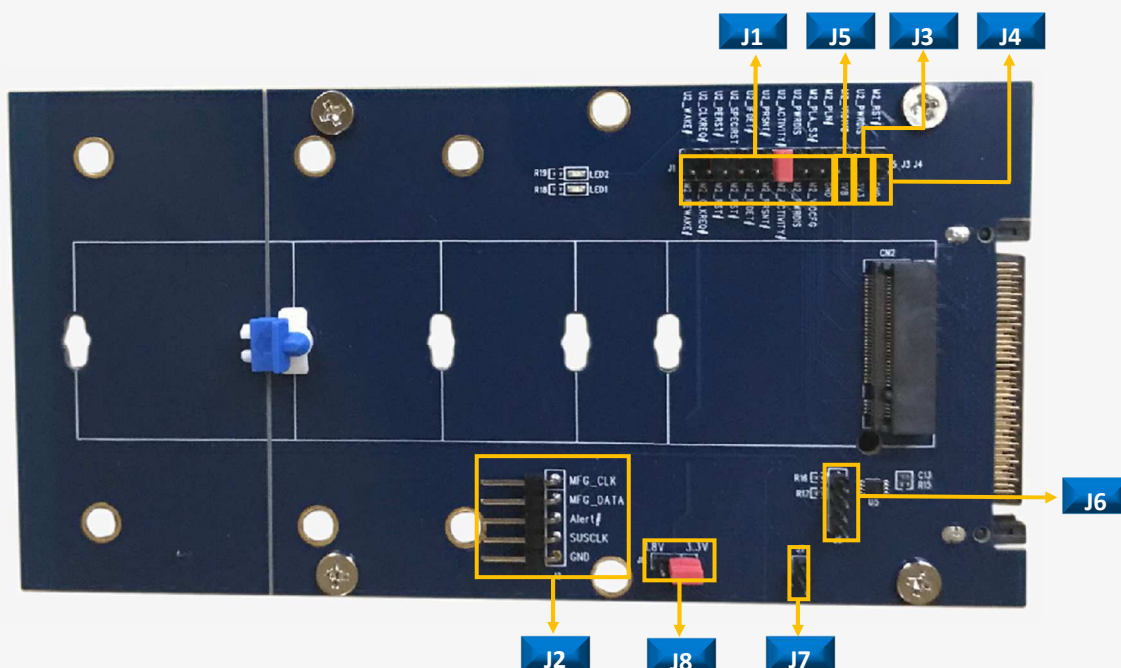


Hardware Specification

Model	PCI5-AD-U2M2-04
PCBA Physical Dimension	69mm(W) x 104mm(L), not including V-cut and supports up to 2280 M.2 SSDs. 69mm(W) x 134mm(L), including V-cut and supports up to 22110 M.2 SSDs. Thickness .063" +/- 0.008" (1.6mm +/- 0.2mm)
LEDs	LED1: Blue , Power LED. LED2: Green , M.2 Activity LED.
M.2 support	2230/2242/2260/2280/22110



Functions of Headers



Headers	Descriptions																				
J8	Pin1&2 ON: Set the pull up to be 1.8V for M.2 side-band signals. Pin2&3 ON: Set the pull up to be 3.3V for M.2 side-band signals. Note: Side-band signals include M2_WAKE# and M2_PERST#.	<table><tr><th>Pins in Header</th><th>Signals</th></tr><tr><td>1</td><td>1.8V</td></tr><tr><td>2</td><td>M2_VIO</td></tr><tr><td>3</td><td>3.3V</td></tr></table>		Pins in Header	Signals	1	1.8V	2	M2_VIO	3	3.3V										
		Pins in Header	Signals																		
		1	1.8V																		
		2	M2_VIO																		
3	3.3V																				
J2	<u>For M.2 MFG SMBus accessing.2</u>																				
	<table><tr><th>Pins in Header</th><th>Signals</th><th>Pins in M.2 connector</th></tr><tr><td>1</td><td>MFG_CLK</td><td>58</td></tr><tr><td>2</td><td>MFG_DATA</td><td>56</td></tr><tr><td>3</td><td>M2_ALERT#</td><td>44</td></tr><tr><td>4</td><td>M2_SUSCLK</td><td>68</td></tr><tr><td>5</td><td>GND</td><td></td></tr></table>			Pins in Header	Signals	Pins in M.2 connector	1	MFG_CLK	58	2	MFG_DATA	56	3	M2_ALERT#	44	4	M2_SUSCLK	68	5	GND	
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	2	MFG_DATA	56																		
	3	M2_ALERT#	44																		
4	M2_SUSCLK	68																			
5	GND																				
J4	ON: Assert M.2 PERST# signal. OFF: De-assert M.2 PERST# signal.	<table><tr><th>Pins in Header</th><th>Signals</th><th>Pins in M.2 connector</th></tr><tr><td>2</td><td>GND</td><td></td></tr><tr><td>1</td><td>M2_PERST#</td><td>50</td></tr></table>		Pins in Header	Signals	Pins in M.2 connector	2	GND		1	M2_PERST#	50									
		Pins in Header	Signals	Pins in M.2 connector																	
		2	GND																		
1	M2_PERST#	50																			
J3	ON: Force U.2 power disable. OFF: Force U.2 power enable.	<table><tr><th>Pins in Header</th><th>Signals</th><th>Pins in M.2 connector</th></tr><tr><td>2</td><td>GND</td><td></td></tr><tr><td>1</td><td>U2_PWRDIS</td><td>P3</td></tr></table>		Pins in Header	Signals	Pins in M.2 connector	2	GND		1	U2_PWRDIS	P3									
		Pins in Header	Signals	Pins in M.2 connector																	
		2	GND																		
1	U2_PWRDIS	P3																			



Headers	Descriptions			
J5	ON: Provide 1.8V to M.2 VIO 1.8V	Pins in Header	Signals	Pins in M.2
	OFF: M.2 VIO 1.8V to be floating	1	1.8V	
		2	M2_VIO1V8	22
J6	<u>For M.2 SMBus accessing.</u>			
	Pins in Header	Signals	Pins in M.2	
	1	GND		
	2	M2_ALERT#	44	
	3	M2_SMDAT	42	
	4	M2_SMCLK	40	
Note: There is a I2C level shifter to translate the 3.3V SMBus which sending from golden finger to 1.8V SMBus in M.2 connector.				
M.2 ALERT# is 1.8V signal level also.				
J7	ON: Disable 12V to 3.3V switching power for M.2			
	OFF: Enable 12V to 3.3V switching power for M.2			



Headers	Descriptions																																																																
	<table><tr><th>Pins in Header</th><th>Signals</th><th>Pins in M.2 connector</th><th>Pins in Header</th><th>Signals</th><th>Pins in U.2 or M.2 connector</th></tr><tr><td>1</td><td>M2_WAKE#</td><td>M2_54</td><td>2</td><td>U2_WAKE#</td><td>U2_P1</td></tr><tr><td>3</td><td>M2_CLKREQ#</td><td>M2_52</td><td>4</td><td>PE_CLKREQ#</td><td>U2_E4</td></tr><tr><td>5</td><td rowspan="2">M2_PERST#</td><td rowspan="2">M2_50</td><td>6</td><td>U2_PERST#</td><td>U2_E5</td></tr><tr><td>7</td><td>8</td><td>U2_SPCIERST</td><td>U2_P2</td></tr><tr><td>9</td><td>M2_IFDET#</td><td>M2_69</td><td>10</td><td>M2_PRSNT#</td><td>M2_1</td></tr><tr><td>11</td><td>M2_PRSNT#</td><td>M2_1</td><td>12</td><td>U2_PRSNT#</td><td>U2_P10</td></tr><tr><td>13</td><td>M2_ACTIVITY#</td><td>M2_10</td><td>14</td><td>U2_ACT#</td><td>U2_P11</td></tr><tr><td>15</td><td>M2_PWRDIS</td><td>M2_6</td><td>16</td><td>U2_PWRDIS</td><td>U2_P3</td></tr><tr><td>17</td><td>M2_VIOCFG</td><td>M2_73</td><td>18</td><td>M2_PLA_S3#</td><td>M2_30</td></tr><tr><td>19</td><td>GND</td><td></td><td>20</td><td>M2_PLN#</td><td>M2_8</td></tr></table> Pin1&2 ON: connect the WAKE# signals between U2 and M.2. Pin3&4 ON: connect the CLKREQ# signals between U2 and M.2. Pin13&14 ON: connect the LED activity# signals between U2 and M.2. Note1 : There is a signal buffer between Pin5&7(M2_PERST#) and Pin6(U2_PERST#) of J1. Can't have jumper short on Pin5&7 and Pin6, otherwise, M2_PERST# signal will be latch off. Note2: M2_IFDET# is connected to M.2 connector Pin69, it is CONFIG_1. L=GND for SATA SSD H=NC for PCIe SSD Note3: M2 PRSNT# is connected to U2_IFDET# in design. A M.2 SSD attached, it will drive U2_IFDET# to low. if no M.2 SSD attached, U2_IFDET# asserts high.	Pins in Header	Signals	Pins in M.2 connector	Pins in Header	Signals	Pins in U.2 or M.2 connector	1	M2_WAKE#	M2_54	2	U2_WAKE#	U2_P1	3	M2_CLKREQ#	M2_52	4	PE_CLKREQ#	U2_E4	5	M2_PERST#	M2_50	6	U2_PERST#	U2_E5	7	8	U2_SPCIERST	U2_P2	9	M2_IFDET#	M2_69	10	M2_PRSNT#	M2_1	11	M2_PRSNT#	M2_1	12	U2_PRSNT#	U2_P10	13	M2_ACTIVITY#	M2_10	14	U2_ACT#	U2_P11	15	M2_PWRDIS	M2_6	16	U2_PWRDIS	U2_P3	17	M2_VIOCFG	M2_73	18	M2_PLA_S3#	M2_30	19	GND		20	M2_PLN#	M2_8
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